REMARKS/ARGUMENTS

Claims 1-20 are pending. Claims 1, 2, 6, 7, 10, 11, 12, 12, 15, and 16 have been amended. New claims 19 and 20 have been added. No new matter has been added.

Claim 1 was objected to for informalities. Claim 1 has been amended. Claims 7 and 16 were rejected under 35 U.S.C. § 112, second paragraph. Claims 7 and 16 have been amended.

Claims 1-4, 6-13, and 15-18 were rejected under 35 U.S.C. § 102(e) as being anticipated by Tran et al. Applicants traverse the rejection. Claim 1 is directed to forming a contact plug in a semiconductor device. The claimed embodiment provides the semiconductor device with an improved refresh time by providing the dopant concentration profile in the plug ion-implantation regions with a reduced slope (see page 4, lines 19 to page 5, line 9). By providing such a dopant concentration profile, it is possible to suppress the width of a depletion layer from being decreased. This makes it possible to mitigate the concentration of electric field at the cell junction and improve the refresh time of the device. The claim recites:

> 1. A method for forming contact plugs on active regions of a semiconductor device, the method comprising:
>
> forming a plurality of gate lines on a substrate;
>
> implanting first dopants of first conductivity type into the substrate using the gate lines as a mask to form a plurality of cell junctions, each gate line being provided between two cell junctions;
>
> forming a buffer layer over the cell junctions; and
>
> implanting second dopants of first conductivity type through the buffer layer and into the cells junctions using a first energy level to form a plurality of plug ion-implantation regions, the plug ion-implantation regions being configured to receive the contact plugs;
>
> implanting the second dopants of first conductivity type through the buffer layer and into the cell junctions using a second energy level that is different from the first energy level to form the plug ion-implantation regions; and
>
> forming a well of second conductivity type within the substrate, wherein the cell junctions and the plug ion-implantation regions are defined within the well,

wherein the buffer layer is configured to enable a higher implantation energy to be used to implant the second dopants, so that a concentration profile of the second dopants has a reduced slope.

The claimed embodiment provides the plug ion-implantation region with a dopant concentration profile having a reduced slope, as indicated by Fig. 3. The graph P2 represents an exemplarily dopant concentration profile according to one embodiment of the present invention. The graph P1 represents a dopant concentration profile according to the conventional method. To obtain a dopant concentration profile having a reduced slope, as that of the graph P2 in Fig. 3, the claimed embodiment implants the second dopants via the buffer layer and also uses first and second implantation energy levels.

Tran discloses a method for forming a double LDD regions and does not appreciate the need for suppressing the width of depletion layer between the well and cell junction from decreasing. Tran does not disclose using a buffer layer to obtain a dopant concentration profile having a reduced slope. Similarly, it does not disclose using two different implantation energy levels to form the plug ion-implantation region to obtain a dopant concentration profile having a reduced slope. In one section, Tran discloses forming a dielectric layer 72 and then performing the implantation steps (col. 10:14-17). In another section, Tran discloses forming a LDD region and then forming the dielectric layer 72 (col. 11:9-12). After forming the dielectric layer 72, heavy ion implant does 44 is performed to form the source and drain regions 36 and 38. Thereafter, second light ion implant dose 56 is performed to form double LDD regions 52, 54. The dielectric layer 72 of Tran does not appear to serve the function of the "buffer layer" of claim 1, i.e., to provide a reduce slope for the dopant concentration profile. Tran does not disclose or suggest other features recited in claim 1. Claim 1 is allowable.

Claim 10 recites, forming a plurality of gate lines on a substrate; forming a plurality of cell junctions by ion-implanting a first dopant type using the gate lines as a mask; forming a buffer layer along a gate line profile; and forming a plurality of plug ion-implantation regions in the cell junctions by ion-implanting a second dopant type into the

substrate under the presence of the buffer layer, wherein the second dopant is implanted through the buffer layer and into the substrate, so that a concentration profile of the second dopant type has a reduced slope; and forming a well within the substrate, wherein the cell junctions and the plug ion-implantation regions are defined within the well. Tran does not disclose or suggest the above recited features. Claim 10 is allowable.

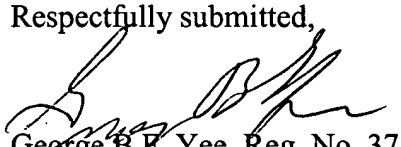
Claims 5 and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran et al. in view of Shirahata et al. Applicants traverse the rejection. Claim 5 depends from claim 1 and claim 14 depends from claim 10. Claims 5 and 14 are allowable at least for the reason their independent claims are allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



George B.F. Yee, Reg. No. 37,478 for
Steve Y. Cho, Reg. No. 44,612

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 650-326-2422
SYC:mcg/km
60591506 v1